Tutorial Proposal:

Advances in time-encoded analog signal processing and data conversion

Presenters: Luis Hernandez, Susana Paton, Enrique Prefasi, Pieter Rombouts

Abstract

The feature size improvement of nanometer CMOS technology represents an enhancement of speed and power consumption for digital circuits but at the expense of analog performance degradation. Time encoding techniques are one of the research trends in analog signal processing to overcome this problem and ease an accurate representation of analog signals within nanometer CMOS chips operating at very low voltage. In essence, time encoding techniques map a continuous time signal into a pulse coded signal. As long as pulse streams are formed of discrete events, some signal processing concepts are needed to bridge both kind of representations. Most time encoding techniques used so far stem from classical pulse modulations such as PWM, PPM and from non uniform sampling schemes. These techniques are known from a signal processing point of view since long ago, but its particular application may not be familiar to analog circuit designers. This tutorial will explore the basics of time encoding techniques and especially, its application to data conversion.

An introductory presentation will review the signal processing concepts involved in time encoding techniques and its implications when applied to CMOS circuit design. A second presentation will discuss the design of continuous time sigma delta converters that rely on time encoding to replace multibit internal ADCs and DACs. This presentation will cover both system and circuit level aspects. Finally, we will show the recent advances in time encoded signal processing using mostly digital elements such as gated and voltage controlled ring oscillators, variable delay gates and asynchronous digital circuitry.

Proposed schedule

9h00 - 10h00 Introduction to Time Encoded Signal Processing (PR)

10h00 - 11h00 Design of continuous time sigma delta modulators with time encoded quantizers (SP)

11h00 - 11h30 Coffee break

11h30 - 12h15 CMOS Circuit design for time encoded analog signal processing (EP)

12h15 - 13h00 Time encoded signal processing using mostly digital circuitry (LH)

Presenter short CV

Luis Hernandez (M'98) received the M.S. and Ph.D., degrees in telecommunication engineering from the Polytechnic University of Madrid, Spain, in 1990 and 1995. From 1996 to 1997, he was a research associate at Oregon State University, Corvallis, where his research focused on sigma-delta data converters. In 1997, he joined the Electronics Department of Carlos III University in Madrid, where he is currently Department Head and Associate Professor. His research interests are low pass and band pass sigma delta modulators, mismatch shaping algorithms and circuits and time encoded systems theory. He has coauthored more than 50 publications and holds 13 Patents. He is currently member of the IEEE Analog Signal Processing Technical Committee (ASPTC) and Associate Editor of Transactions of Circuits and Systems II.

Susana Paton (M'05) received the M.Sc. and the Ph.D. in electrical engineering from the Universidad Carlos III, Madrid, Spain, in 1998 and 2005, where she is currently Associate Professor. From 2001 to 2009 she was a part-time consultant for Infineon Technologies Austria, collaborating in the design of low power continuous time Sigma-Delta converters for high speed applications. Her PhD thesis was honored with the "Doctoral Exceptional Award" by the Carlos III University in 2007. Her research interests are circuits and systems theory, A/D converters and Sigma-Delta modulation. She is coauthor of more than 30 publications and holds 6 patents.

Enrique Prefasi (M'08) was born in Madrid, Spain, in 1978. He received the M.Sc. and the Ph.D. in Electrical Engineering from the Carlos III University, Madrid, Spain, in 2003 and 2008, respectively. Since 2003 he has been with the Electronics Technology Department of Carlos III University, Madrid, Spain, where he is currently an Assistant Professor. His Ph.D. thesis, about high speed Band-Pass Continuous-Time Sigma-Delta Modulators, was honored with the "Doctoral Exceptional Award" by the Carlos III University in 2008. Since 2004 he has been a part-time consultant for Lantiq AG Austria (former Infineon AG Austria), collaborating in the design of Sigma-Delta converters for high speed applications. In 2009 he did a postdoctoral research stay at IMEC, Leuven, Belgium, where he focused on the design of ultra-low power ADCs for Biomedical sensors under Human++ project. During this period he has participated in

several RTD projects financed with private and public funds, leading some of them. He has been also the author and co-author of more than 25 papers and patent applications, receiving in 2010 the "ESSCIRC Best Paper Award" for the paper entitle "A 0.08 mm2, 7mW Time-Encoding Oversampling Converter with 10 bits and 20MHz BW in 65nm CMOS". Currently, his research interests are analog-to-digital converters, sigma-delta modulators and analog circuit design for low-power low-voltage applications.

Pieter Rombouts was born in Leuven, Belgium in 1971. He obtained the Ir. degree in applied physics and the Dr. degree in electronics from Ghent University in 1994 and 2000 respectively. The title of his doctoral dissertation was "Error correction for D/A- and A/D-converters" (in dutch). Since 1994 he has been with the Electronics and Information Systems Department of Gent university where he is a professor of analog electronics since 2005. His technical interests are signal processing, circuits and systems theory and analog circuit design with a special focus on the use of system-level techniques to tackle problems that are inherent to circuit imperfections. He has cooperated in several (industrial) research projects in this area and has authored multiple journal papers. He currently serves as an Associate Editor of Transactions of Circuits and Systems II.

Presenter's publications related to the conference

[1] Hernandez Corporales, L.; Prefasi, E.; Pun, E.; Paton, S."A 1.2-MHz 10-bit Continuous-Time Sigma–Delta ADC Using a Time Encoding Quantizer", Transactions on Circuits and Systems II, Jan. 2009, Volume 56, Issue 1, Page(s): 16-20

[2] Hernandez, L.; Pun, E.; Prefasi, E.; Paton, S. "A Continuous time sigma-delta modulator based on binary weighted charge balance" Electronics Letters. Volume 45, Issue 9, April 23 2009 Page(s):458 - 460.

[3] Prefasi, E.; Hernandez, L.; Paton, S.; Wiesbauer, A.; Gaggl, R.; Pun, E.; "A 0.1 mm2 , Wide Bandwidth Continuous-Time Sigma Delta ADC Based on a Time Encoding Quantizer in 0.13um CMOS" Solid-State Circuits, IEEE Journal of , Volume 44, Issue 10, Oct. 2009 Page(s):2745 - 2754

[4] Hernandez , L.; Prefasi, E.; "Continuous time ΣΔ modulator based on digital delay loop and time quantisation," Electronics Letters , vol.46, no.25, pp.1655 -1656, December 9 2010

[5] Hernandez , L.; Paton, S.; Prefasi, E.; , "VCO-based sigma delta modulator with PWM precoding," Electronics Letters , vol.47, no.10, pp.588 -589, May 12 2011

[6] Prefasi, E.; Paton, S.; Hernandez, L.; , "A 7 mW 20 MHz BW Time-Encoding Oversampling Converter Implemented in a 0.08 mm2 65 nm CMOS Circuit," Solid-State Circuits, IEEE Journal of , no.99, 2011

[7] Hernández, L.; , "VCO based multi-stage noise shaping ADC," Electronics Letters , vol.48, no.4, pp.206-208, February 16 2012

[8] B. De Vuyst and P. Rombouts, “A 5-MHz 11-Bit Self-Oscillating sigma delta modulator with a delay-based phase shifter in 0.025 mm(2),” IEEE J. Solid-State Circ., vol. 46, no. 8, p. 1919-1927, 2011.

[9] B. De Vuyst, P. Rombouts, and G. Gielen, “A rigorous approach to the robust design of continuous-time ΣΔ modulators,” IEEE Trans. Circuits and Syst.-I, vol. 58, no. 12, p. 2829-2837, 2011.

[10] Xinpeng Xing, M. De Bock, P. Rombouts, and G. Gielen, “A 40MHz 12bit 84.2dB-SFDR continuous-time delta-sigma modulator in 90nm CMOS,” in IEEE Asian solid-state circuits conference, Proceedings, p. 249-252, IEEE, 2011.

[11] P. Woestyn, P. Rombouts, X. Xing, and G. Gielen,``{A selectable-bandwidth 3.5 mW, 0.03 mm(2) self-oscillating Sigma Delta modulator with 71 dB dynamic range at 5 MHz and 65 dB at 10 MHz bandwidth},'' Analog Integrated Circuits And Signal Processing, vol. 72, pp. 55-63, Jul. 2012.

[12] L. Bos, G. Vandersteen, P. Rombouts, A. Geis, A. Morgado, Y. Rolain, G. Van der Plas, and J. Ryckaert, “Multirate cascaded discrete-time low-pass ΔΣ modulator for GSM/Bluetooth/UMTS,” IEEE J. Solid-State Circ., vol. 45, no. 6, p. 1198-1208, 2010